WHAT IS CLAIMED IS:

1. A program translator comprising:

instruction exchanging means for exchanging one of instructions included in a program for another instruction, the latter instruction specifying an operation equivalent to that specified by the former instruction, the latter instruction designating, as a target of the operation, an execution unit that is different from an execution unit designated as a target by the former instruction; and

instruction parallelizing means for placing the instructions in the program, in which the former instruction has been exchanged for the latter instruction by the exchanging means, at such locations as being parallelly executable by a processor.

2. The program translator of Claim 1, wherein the instruction exchanging means comprises:

equivalent instruction storage means for storing multiple instructions that specify equivalent operations but designate mutually different execution units as targets of the operations;

instruction identifying means for identifying at least one of the instructions included in the program with one of the instructions stored on the storage means; and

instruction replacing means for replacing the at least

one instruction, which has been identified by the identifying means, with another one of the instructions that is also stored on the storage means but is different from the at least one instruction.

3. The program translator of Claim 1, further comprising parallelism-level calculating means for calculating a parallelism level of the instructions that have been parallelized by the parallelizing means.

4. The program translator of Claim 1, wherein the instruction exchanging means comprises:

equivalent instruction set storage means for storing multiple instruction sets specifying mutually equivalent operations, wherein if two of the instruction sets each designate the same set of execution units as targets of their operations in the same order, these two instruction sets belong to the same group of instructions;

instruction subset identifying means for identifying a subset of the program with one of the instruction sets stored on the storage means;

instruction group selecting means for selecting an instruction group that is different from a group to which the instruction set, identified by the identifying means with the instruction subset, belongs; and

instruction set replacing means for replacing the instruction subset, which has been identified by the identifying means, with an instruction set included in the instruction group selected by the selecting means.

5. A program translator comprising:

instruction parallelizing means for generating a set of parallelized instructions by placing instructions at such locations as being parallelly executable by a processor;

equivalent instruction storage means for storing multiple instructions that specify equivalent operations but designate mutually different execution units as targets of the operations;

no-operation instruction finding means for finding a no-operation instruction from the parallelized instructions located in a predetermined range of the parallelized instruction set;

substitute instruction selecting means for selecting, if one of the parallelized instructions including the no-operation instruction found is the same as one of the instructions stored on the storage means, a substitute one of the instructions, which is also stored on the storage means but is different from the instruction included in the parallelized instructions; and

instruction replacing means for replacing the instruction

included in the parallelized instructions with the substitute instruction selected by the selecting means.

6. The program translator of Claim 5, further comprising:

effective range searching means for searching the parallelized instruction set for a subset of instructions, which does not cause register conflict with any of the parallelized instructions; and

second no-operation instruction finding means for finding a no-operation instruction from parallelized instructions included in the instruction subset that has been found by the searching means,

wherein the replacing means replaces the no-operation instruction, which has been found by the second finding means, with the instruction that has been selected by the selecting means.

7. A processor comprising:

a first execution unit;

a second execution unit; and

instruction parallelizing/executing means for executing two instructions, which designate the first execution unit as a target, in parallel by allocating one of the two instructions to the second execution unit.

8. The processor of Claim 8, wherein the parallelizing/executing means comprises:

instruction recognizing means for recognizing the two instructions as instructions both designating the first execution unit as the target;

allocation changing means for allocating one of the two instructions that designate the first execution unit as the target to the second execution unit; and

parallel executing means for executing the two instructions in parallel.

9. A processor comprising:

a first execution unit, on which an operation will be performed in a first number of cycles;

at least one second execution unit, on which an operation will be performed in a second number of cycles, the second number being smaller than the first number;

instruction recognizing means for recognizing a predetermined instruction as an instruction designating the first execution unit as a target of the operation; and

instruction exchanging means for exchanging the predetermined instruction that has been recognized by the recognizing means with at least one instruction that specifies an operation equivalent to that specified by the instruction and designates the second execution unit as a target.

10. The processor of Claim 9, wherein exchanging means comprises:

instruction set searching means for searching for an instruction set that specifies an operation equivalent to that specified by the predetermined instruction;

comparing means for comparing a point in time execution of the instruction set found by the searching means is completed to a point in time execution of the predetermined instruction is completed; and

instruction replacing means for replacing, if the comparing means has determined that the execution of the instruction set will be completed earlier than that of the predetermined instruction, the predetermined instruction with the instruction set.